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Description

MAGNETIC RANDOM ACCESS MEMORY AND METHOD OF FABRICATING THEREOF

BACKGROUND OF INVENTION

[0001] The present invention relates generally to magnetic memory devices and, more particularly, to a process sequence of fabricating magnetic random access memory (MRAM) devices.

[0002] Magnetic (or magneto-resistive) random access memory (MRAM) is a promising technology in the development of non-volatile random access memory that could begin to replace the existing dynamic random access memory (DRAM) as the standard memory for computing devices. The use of MRAM as a non-volatile RAM will eventually allow for "instant on" systems that come to life as soon as the system is turned on, thus saving the amount of time needed for a conventional PC, for example, to transfer boot data from a hard disk drive to volatile DRAM during

system power up.

[0003] A magnetic memory element (also referred to as a tunneling magneto-resistive, or TMR device) includes a structure having ferromagnetic layers separated by a non-magnetic layer, and arranged into a magnetic tunnel junction (MTJ). Digital information is stored and represented in the memory element as directions of magnetization vectors in the magnetic layers. More specifically, magnetic vectors in one magnetic layer (also referred to as a reference layer) are magnetically fixed or pinned, while the magnetization direction of the other magnetic layer (also referred to as a "free" layer) may be switched between the same direction and the opposite direction with respect the fixed magnetization direction of the reference layer. The magnetization directions of the free layer are also known "parallel" and "antiparallel" states, wherein a parallel state refers to the same magnetic alignment of the free and reference layers, while an antiparallel state refers to opposing magnetic alignments therebetween.

[0004] Depending upon the magnetic state of the free layer (parallel or antiparallel), the magnetic memory element exhibits two different resistances in response to a vertically applied current with respect to the TMR device. The

particular resistance of the TMR device thus reflects the magnetization state of the free layer, wherein resistance is "low" when the magnetization is parallel, and "high" when the magnetization is antiparallel. Accordingly, a detection of changes in resistance allows an MRAM device to provide information stored in the magnetic memory element (i.e., a read operation). In addition, an MRAM cell is written to through the application a bi-directional current in a particular direction, in order to magnetically align the free layer in a parallel or antiparallel state.

[0005] A practical MRAM device integrates a plurality of magnetic memory elements with other circuits such as, for example, control circuits for the magnetic memory elements, comparators for detecting the states in the magnetic memory elements, input/output circuits, etc. As such, there are certain microfabrication processing difficulties to be overcome before high capacity/density MRAM products become commercially available. For example, in order to reduce the power consumption of the device, CMOS switching technology is desirable. As is known in the art, various CMOS processing steps (such as depositing dielectric and metal layers and annealing implants) are carried out at relatively requires high temperatures (e.g., in excess of

300E C). On the other hand, magnetic layers employ ferromagnetic material, such as CoFe and NiFeCo, that requires processing temperatures below 300E C in order to prevent intermixing of magnetic materials. Thus, the magnetic memory elements need to be fabricated at a different stage after CMOS processing.

[0006] Moreover, magnetic memory elements contain components that are easily oxidized and also sensitive to corrosion. To protect magnetic memory elements from degradation and keep the performance and reliability of the MRAM device, a passivation layer is typically formed thereupon. In addition, a magnetic memory element includes very thin layers, some of them on the order tens of angstroms thick. Because the performance of the magnetic memory element is particularly sensitive to the surface conditions on which magnetic layers are deposited, it is desirable to maintain a relatively flat surface to prevent the characteristics of an MRAM device from degrading.

[0007] Notwithstanding the above described processing variations between ferromagnetic materials and conventional DRAM elements, it is desirable to be able to simplify the MRAM fabrication process and increase the compatibility thereof with conventional back-end-of-line (BEOL), e.g.

copper, metallization techniques.

SUMMARY OF INVENTION

[0008] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for forming an interconnect structure in a magnetic random access memory (MRAM) device. In an exemplary embodiment, the method includes defining a magnetic stack layer on a lower metallization level, the magnetic stack layer including a non-ferromagnetic layer disposed between a pair of ferromagnetic layers. A conductive hardmask is defined over the magnetic stack layer, and selected portions of the hardmask and the magnetic stack layer, are then removed, thereby creating an array of magnetic tunnel junction (MTJ) stacks. The MTJ stacks include remaining portions of the magnetic stack layer and the hardmask, wherein the hardmask forms a self aligning contact between the magnetic stack layer and an upper metallization level subsequently formed above the MTJ stacks.

[0009] In another aspect, a magnetic random access memory (MRAM) device includes a magnetic stack layer formed on a lower metallization level, the magnetic stack layer having a non-ferromagnetic layer disposed between a pair of ferromagnetic layers. A conductive hardmask is formed

over the magnetic stack layer, and an array of magnetic tunnel junction (MTJ) stacks is created by the removal of selected portions of the hardmask and the magnetic stack layer. The MTJ stacks include remaining portions of the magnetic stack layer and the hardmask, wherein the hardmask forms a self aligning contact between the magnetic stack layer and an upper metallization level formed above the MTJ stacks.

Brief Description of Drawings

[0010] Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

[0011] Figures 1-11 are sectional views of processing steps in conjunction with a method for forming a magnetic random access memory (MRAM) device, in accordance with an embodiment of the invention, in which a plurality of magnetic tunnel junction (MTJ) stacks includes a metal hardmask layer thereupon.

Detailed Description

[0012] Disclosed herein is an improved process sequence of fabricating magnetic random access memory (MRAM) devices wherein, among other aspects, a metal hardmask is formed over a plurality of magnetic tunnel junction (MTJ)

stacks thereby providing a self-aligned contact between the stacks and subsequent upper metallization lines formed thereupon. The metal hardmask also serves as an etch stop layer for subsequent dual damascene processing steps used in the formation of the upper metallization lines and vias connecting the upper metallization lines to lower metallization lines (on which the MTJ stacks are formed).

[0013] Referring initially to Figure 1, there is shown a sectional view of the formation of the MTJ stacks of an MRAM device 100. Prior to the stack formation, the fabrication of the MRAM structure 100, up to the second level of metallization, is implemented in accordance with well known fabrication processes. The lower level, or front end of line (FEOL) structures, include transistor device 102 formed upon a silicon or other suitable substrate 104, along with isolation regions 106. An interlevel dielectric layer 108, such as SiO2, is used to insulate the active substrate devices (e.g., transistor 102) from a first metallization layer M1, except where the transistor 102 is connected to M1 by contact area 110.

[0014] The first metallization layer M1 is formed within a liner or barrier layer 112 (e.g., tantalum/tantalum nitride) which in

turn is formed upon a nitride layer 114 on a first interlevel dielectric (ILD) layer 108. A second interlevel dielectric layer 115 is also formed upon nitride layer 114. Further, a second metallization layer M2 (and liner) is formed upon a third interlevel dielectric layer 116, wherein electrical contact between the first and second metallization layers M1, M2 is achieved through via V1. As with the second interlevel dielectric layer 115, the third interlevel dielectric layer 116 is also formed upon a nitride layer 118.

[0015] Those skilled in the art will appreciate that the first metallization layer M1, as well as the combination of via V1 and second metallization layer M2, may be formed by, for example, by conventional damascene processing and dual damascene processing, respectively. It will also be appreciated that the aforementioned FEOL structures (denoted collectively by 120 in subsequent Figures) are presented by way of example only, and are thus not discussed in further detail hereinafter.

[0016] The MTJ stack formation process begins with the deposition of a magnetic stack layer (collectively denoted by 122) deposited over the M2 lines and the ILD layer 116, and comprising a non-ferromagnetic layer sandwiched between a pair of ferromagnetic layers, allowing for spin-

dependent tunneling. The ferromagnetic material used in the stack layer 122 may include materials such as IrMn, PtMn, CoFe, CoFeB, Ru, Al_2O_3, and NiFe for example. Other types of magnetic material, such as Ni, Co, and various ratios of the compounds mentioned above, may also be used. It should also be noted at this point that the magnetic stack layer 122 need not necessarily be formed upon M2, but could also be formed upon M1 or at a higher metallization level than M2.

[0017] Once the magnetic stack layer 122 is deposited, a metal hardmask layer 124 is then deposited thereupon as shown in Figure 2. In a preferred embodiment, the hardmask layer 124 includes a conductive material such as tantalum, tungsten, titanium, and compounds thereof, such as tantalum nitride or titanium nitride. However, other types of conductive materials can also be used. The hardmask layer 124 is deposited by, for example, physical vapor deposition (PVD), chemical vapor deposition (CVD), or other techniques. In addition, the thickness of the hardmask layer 124 is preferably sufficient to serve as a hardmask for etching of the magnetic stack layer 122.

[0018] After being deposited, the hardmask layer 124 is then lithographically patterned and the resulting photo resist

125 pattern is transferred to the hardmask 124 layer by RIE, for example, as is also shown in Figure 2. In Figure 3, the pattern is also shown transferred into the magnetic stack layer 122 by reactive ion etching (RIE) or ion milling, for example, to define the individual MTJ stacks 126. Once the MTJ stacks 126 are defined, a cap layer 128 is deposited to seal the exposed portions of the M2 surface in subsequent processing steps, as shown in Figure 4. The cap layer 128 may be, for example, a layer of silicon nitride deposited by CVD.

[0019] Referring now to Figure 5, another interlevel dielectric layer 130 is blanket deposited over the cap layer 128, in preparation for the formation of an upper metallization layer (M3) and a via level for interconnection between M2 and M3. Thus, the ILD layer 130 is deposited at a sufficient thickness for by M3 and V2 formation. As a result of the step heights created by the formation of the MTJ stacks 126 (and in particular due to the thickness of the hardmask layer 124), the deposition of ILD layer may result in nonplanarities 132 over the stacks 126. Accordingly, the ILD layer 130 may be planarized by chemical mechanical polishing (CMP) for example, as shown in Figure 6, so long as a sufficient thickness for M3 and V2 is

maintained. Alternatively, a thicker cap layer 128 (i.e., having a cap thickness equal to or greater than the total thickness of the MTJ stacks 126) may deposited and thereafter planarized. Then, the ILD layer 130 may be deposited at a smaller thickness, since it will already be formed at a sufficient planarity.

[0020] Figure 7 illustrates the formation of M3 trenches 134 for a subsequent damascene metal process by lithography, patterning and RIE to transfer the desired pattern from a photo resist layer to ILD layer 130, wherein the cap layer 128 may serve as an etch stop for the M3 trench pattern in certain parts of the pattern. Following the etching of the M3 trenches 134, the remaining resist may either be stripped by cleaning or left in place for the next lithography and etch process in which the via openings 136 for V2 are defined, as shown in Figure 8. As was the case for the definition of the M3 trenches, the cap layer 128 serves as an etch stop layer for the V2 definition. Upon completion of the V2 via opening formation, the remaining resist is stripped by a cleaning step, as shown in Figure 9.

[0021] In Figure 10, the cap layer 128 is removed (by etching, for example) in order to expose the hardmask layer 124 of the MTJ stacks 126, as well as those portions of M2 to be

contacted by the V2 vias. However, as an alternative approach to the steps illustrated in Figures 7 and 8, the V2 openings may be lithographically patterned and etched first, with the cap layer 128 being used as an etch stop layer. Then, the M3 trench lithography and etching may be carried out, followed by the removal of the cap layer 128. In either case, the resulting structure will be the same as that shown in Figure 10. Finally, as shown in Figure 11, the metal fill of V2 and M3, along with subsequent planarization, is carried out in accordance with existing dual damascene processing techniques. This may include, for example, a copper (Cu) liner and seed layer deposition, followed by Cu plating and CMP.

[0022] The formation of the hardmask layer 124 as part of the MTJ stack 126 proves beneficial to the overall BEOL processing of the MRAM device in a number of aspects. First, the hardmask serves to define the MTJ stack 126 and is thus self-aligned to the stack. Second, because the hardmask is purposely made of an electrically conducting material, it ultimately serves as a functional part of the working device as an electrical conduit between the magnetic stack layer 122 and the M3 metallization lines. The conductive nature of the hardmask thereby eliminates the

need for a separate processing level to create the connection to M3 (such as, for example, by a damascene via). The dual function of a hardmask, which itself becomes a self-aligned connective element in the finished device, simplifies the BEOL fabrication. Thus, the BEOL processing of MRAM devices is more enhanced than existing MRAM processing techniques, and is also more simplified and/or compatible as compared with the conventional Cu BEOL processes.

[0023] While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.